WHAT IS CLAIMED IS:

1. A data processing processor including a bus arbitration apparatus for selecting one channel with respect to bus use requests issued from a plurality of channels and allowing the selected channel to use the bus,

said bus arbitration apparatus comprising:

a timer responsive to a bus use request notified with respect to a channel having a high necessity of a real-time processing operation, for counting a count value indicative of bus use permission time given to said channel having the high necessity of the real-time processing operation;

a register for setting either a value larger than a maximum value of the count time of said timer or another value smaller than a minimum value of the count time thereof with respect to a channel having a low necessity of a real-time processing operation; and

a control circuit for comparing the count value of the timer with the value of the register, for the respective channels, and allowing one channel having either a small value or a large value in the comparison result to use the bus at bus arbitration.

2. A data processing processor as claimed in claim 1 wherein:

said data processing processor includes; a CPU interface unit for transmitting/receiving a signal between the own data processing processor and a host

CPU; an image processing unit for executing an on-screen display operation and a two-dimensional graphic calculation process; a video input unit for capturing an external input image; a display unit for synthesizing images with each other to output a synthesized image outside the data processing processor; and a memory interface unit for transmitting/receiving a signal between the own data processing processor and an external storage apparatus;

said memory interface unit includes said bus arbitration apparatus;

said channel having the high necessity of the real-time processing operation corresponds to the respective channels of said CPU interface unit, said image processing unit, and said display unit; and

said channel having the low necessity of the real-time processing operation corresponds to the respective channels of said video input unit and said memory interface unit.

3. A data processing processor as claimed in claim 2 wherein:

said bus is equal to a data bus connected between said external storage apparatus and said interface unit; and

said data bus is connected via the memory interface unit including said bus arbitration apparatus to the respective channels.

4. A data processing processor as claimed in

claim 2 wherein:

said external storage apparatus corresponds to either a DRAM or an SDRAM; and

said memory interface unit further comprises:

a refresh operation requesting circuit for producing a request signal used to execute a refreshing operation of said DRAM, or said SDRAM for a time period during which said display unit does not issue the bus use request.

5. A data processing processor as claimed in claim 4 wherein:

said bus is a data bus connected between said external storage apparatus and said interface unit; and

said data bus is connected via the memory interface unit including said bus arbitration apparatus to the respective channels.

6. A data processing processor including a bus arbitration apparatus for selecting one channel with respect to bus use requests issued from a plurality of channels and for allowing the selected channel to use the bus,

said bus arbitration apparatus comprising:

a first type of timer provided with respect to a channel having a high necessity of a real-time processing operation, and responsive to a bus use request notified with respect to a channel having the high necessity of the real-time processing operation, for counting a count value indicative of bus use

permission time given to said channel having the high necessity of the real-time processing operation;

a second type of timer provided with respect to a channel having a low necessity of a real-time processing operation, and for stopping a counting operation of the own timer with either a value larger than an initial value of the count time of said first type of timer with respect to the channel having the high necessity of the real-time processing operation or a value smaller than said initial value of the count time thereof; and

a control circuit for comparing the count value of the first type timer with the value of the second type timer, for the respective channels, and allowing one channel having either a small value or a large value in the comparison result to use the bus at bus arbitration.

7. A data processing processor as claimed in claim 6 wherein:

said data processing processor includes; a CPU interface unit for transmitting/receiving a signal between the own data processing processor and a host CPU; an image processing unit for executing an on-screen display operation and a two-dimensional graphic calculation process; a video input unit for capturing an external input image; a display unit for synthesizing images with each other to output a synthesized image outside the data processing

processor; and a memory interface unit for transmitting/receiving a signal between the own data processing processor and an external storage apparatus;

said memory interface unit includes said bus arbitration apparatus;

said channel having the high necessity of the real-time processing operation corresponds to the respective channels of said CPU interface unit, said image processing unit, and said display unit; and

said channel having the low necessity of the real-time processing operation corresponds to the respective channels of said video input unit and said memory interface unit.

8. A data processing processor as claimed in claim 7 wherein:

said bus is equal to a data bus connected between said external storage apparatus and said interface unit; and

said data bus is connected via the memory interface unit including said bus arbitration apparatus to the respective channels.

9. A data processing processor as claimed in claim 7 wherein:

said external storage apparatus corresponds to either a DRAM or an SDRAM; and

said memory interface unit further comprising:

a refresh operation requesting circuit for

producing a request signal used to execute a refreshing operation of said DRAM, or said SDRAM for a time period during which said display unit does not issue the bus use request.

10. A data processing processor as claimed in claim 9 wherein:

said bus is a data bus connected between said external storage apparatus and said interface unit; and

said data bus is connected via the memory interface unit containing said bus arbitration apparatus to the respective channels.

11. A data processing processor including a bus arbitration apparatus for selecting one channel with respect to bus use requests issued from a plurality of channels and for allowing the selected channel to use the bus,

said bus arbitration apparatus comprising:

a timer responsive to a bus use request notified with respect to a channel having a high priority order, for counting a count value indicative of bus use permission time given to said channel having the high priority order;

a register for setting either a value larger than a maximum value of the count time of said timer or another value smaller than a minimum value of the count time thereof with respect to a channel having a priority order; and

a control circuit for comparing the count

value of the timer with the value of the register, for the respective channels, and allowing one channel having either a small value or a large value in the comparison result to use the bus at bus arbitration.

12. A data processing processor containing a bus arbitration apparatus for selecting one channel with respect to bus use requests issued from a plurality of channels and for allowing the selected channel to use the bus,

said bus arbitration apparatus comprising:

a first type of timer provided with respect to a channel having a high priority order, and responsive to a bus use request notified with respect to a channel having the high priority order, for counting a count value indicative of bus use permission time given to said channel having the high priority order;

a second type of timer provided with respect to a channel having a low priority order, and for stopping a counting operation of the own timer with either a value larger than an initial value of the count time of said first type of timer with respect to the channel having the high priority order or a value smaller than said initial value of the count time thereof; and

a control circuit for comparing the count value of the first type timer with the count value of the second type timer, for the respective channels, and

allowing one channel having either a small value or a large value in the comparison result to use the bus at bus arbitration.